DRONACHARYA COLLEGE OF ENGINEERING

KHENTAWAS, FARRUKHNAGAR, GURGAON, HR

Department: ECE Department

Lecture Plan with Asssignment questions

Subject with code: VHDL&Digital Design(PEC-ECE-312G)

Name of Faculty with designation : Dr. Ekta Thakur, Assistant Professor

S.No.	Month	Date & Day	Sem-Class	Unit	Topic/Chapter covered	Write Lecture Wise Questions
1	May	1	VI ECE	I	Introduction to computer aided design for digital system,hardare description language,introduction to VHDL,	Q1) Question related to digital system Q2) Question related to hardare description language
2	May	2	VI ECE	I	data objects, classes,	Q1) Question related to data objects Q2) Question related to classes
3	May	3	VI ECE	I	data types, operators,	Q1) Question related to operators Q2) Question related to data types
4	June	4	VI ECE	I	overloading logical operators	Q1) Question related to overloading Q2) Question related to operators
5	June	5	VI ECE	I	types of delay, entity and architecture declaration,	Q1) Complexity analysis of delay Q2) Complexity analysis of architecture declaration
6	June	6	VI ECE	I	introduction to behavioral data flow	Q1) Complexity analysis of data flow Q2) Complexity analysis of behavioral
7	June	7	VI ECE	II	structural models	Q1) Complexity analysis of structural Q2) Question related to digital system
8	June	8	VI ECE	II	assignmenys statements	Q1) Complexity analysis of assignments statments
9	June	9	VI ECE	II	sequential statements	Q1) Programes Q2) Programes
10	June	10	VI ECE	II	process condititional statements,	Q1) Complexity analysis of process condititional statements, Q2) Programes

11	June	11	VI ECE	II	case statements,Array and loops,	Q1) Programes Q2) Programes
12	June	12	VI ECE	II	resolution functions, packages and libraries,	Q1) Programes Q2) Programes
13	July	13	VI ECE	II	concurrent statements	Q1) Programes Q2) Programes
14	July	14	VI ECE	II	subprograms:application of function and procedures,	Q1) Complexity analysis of data flow Q2) Complexity analysis of behavioral
15	July	15	VI ECE	III	structural modelling component declaration,	Q1) Complexity analysis of modelling Q2) Complexity analysis of declaration
16	July	16	VI ECE	III	structural layout and generics,VHDL Models ,	Q1) Complexity analysis of generics Q2) Complexity analysis of models
17	July	17	VI ECE	III	concurrent statements	Q1) Complexity analysis of concurrents Q2) Program
18	July	18	VI ECE	III	such as Multiplexers, demultiplexers	Q1) Complexity analysis of multiplexerrs Q2) Complexity analysis of demultiplexers
19	July	19	VI ECE	III	decoders,code converters,comparators	Q1) Complexity analysis of decoders Q2) Complexity analysis of comparators
20	July	20	VI ECE	III	Implementation of boolean function etc,...,VHDL Models	Q1) Complexity analysis of data flow Q2) Complexity analysis of behavioral
21	July	21	VI ECE	III	Simulation of sequential circuits,counters etc..	Q1) Complexity analysis of counters Q2) Complexity analysis of circuits
22	July	22	VI ECE	IV	Basic components of a computer	Q1) Complexity analysis of keyboarbs Q2) Complexity analysis of computer
23	August	23	VI ECE	IV	specification,architecture of microcomputer system	Q1) Numerical based on architectureof microcomputer Q2) program
24	August	24	VI ECE	IV	Implementation of of simple microcomputer system	Q1) Numerical based on microsystem Q2) program
25	August	25	VI ECE	IV	VHDL Programmable logic devices: ROM,PLAs,PALs	Q1) Numerical based on ROM Q2) program
26	August	26	VI ECE	IV	PALs	Q1) Numerical based on PAL Q2) program

27	August	27	VI ECE	IV	GAL,PEEL	Q1) Numerical based on GAL Q2) program
28	August	28	VI ECE	IV	CPLD	Q1) Numerical based on CPLD Q2) program
29	August	29	VI ECE	IV	FPGA	Q1) Numerical based on FPGA Q2) program
30	August	30	VI ECE	IV	Design implementation using CPLDs	Q1) Numerical based on CPLDs Q2) program
31	August	31	VI ECE	IV	Design implementation using FPGAs	Q1) Numerical based on FPGAs Q2) Numerical